REMARKS

Claims 7, 9, 14, 16, 28, 30, 36, and 38 have been amended. No claims have been cancelled or added. Thus, claims 1-17, 19-41, 43-49, and 51 are pending.

Claims 19-21 have been allowed. Allowable subject matter has been identified in claims 7-10, 14-17, 28-31, and 36-39, however, these claims stand objected to as being dependent upon a rejected base claim. Applicant's representative is grateful for the indication of allowable subject matter. Claims 7, 9, 14, 16, 28, 30, 36, and 38 have been rewritten as independent claims incorporating the limitations of their respective base and intervening claims. Accordingly, the objection to claims 7-10, 14-17, 28-31, and 36-39 should be withdrawn.

The present invention is directed to the connection of a massively parallel processor array to a memory array in a bit serial manner to effect a byte wide data reorganization. Referring to Fig. 2, some computer systems include a main memory 12 which is coupled to both a system CPU 10 via a traditional multi-bit wide bus as well as a massively parallel processing array 14 coupled via a plurality of high speed links to the same main memory 12. The massively parallel processing array 14 typically includes a large plurality of processing elements (PEs) which are arranged as a grid (Fig. 3).

As illustrated in Fig. 4, the plurality of PEs (16a-16n) are typically coupled to the main memory 12 via a corresponding plurality of 1-bit wide data connections 24. Typically, the PEs are designed to read and write data in a vertical direction 30 of the main memory 12. See application at page 4. On the other hand, the CPU 10 of the computer system, accesses the main memory 12 using a traditional multi-bit wide CPU-memory bus and reads and writes the main memory 12 in a horizontal direction 32. See application at page 5. Prior art computer systems therefore must store data in the main memory in accordance with a data format consistent with one direction (e.g., vertically for efficient access by the array of PEs) and convert the data into another data format consistent with the other direction (e.g., horizontally, for the CPU to transfer between data between main

memory and external devices) as necessary depending on what device is accessing the memory. Id. This conversion process may be performed by the PEs, however, the need to convert data format is overhead and reduces the processing throughput of the computer system.

In the present invention the need for the PEs to perform data format conversion is eliminated. Data is stored in the main memory in accordance to one format and if the data must be accessed in another format the conversion is performed "on the fly" by a connection circuit coupled between the PEs and the main memory. See Fig. 5-6. A connection circuit is associated with each PE and includes a plurality of memory buffer registers. The connection circuit can operate in both the horizontal and vertical access modes. In the horizontal access mode, the memory bits are selected so that all bits of a given byte are stored in the same PE (i.e., each set of buffer registers associated with a respective PE contains one byte as seen by the CPU 10 or an external device). In the vertical access mode, each set of buffer registers contains the successive bits at successive locations in the memory corresponding to that PE's position in the memory word. The selection is achieved utilizing a multiplexer on the input to the register and a pair of tri-state drives which drive each data line.

Accordingly, claims 1 and 22 recite:

> a circuit coupled between said main memory and said plurality of processing elements, said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements.

Claim 11 and 33 recite:

> a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements ... wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time.

Claim 41 recites:

> providing a plurality of data bits in a serial manner from said processing element to a data circuit; passing said data through said data circuit; and writing said data to said memory device, wherein said data circuit passes said data directly to said memory device in a horizontal mode

And claim 48 recites:

> providing a plurality of data bits from said memory device to a data circuit; passing said data through said data circuit; and outputting said data to said processing element in a serial manner, and wherein at least a portion of said data is stored in said memory device in a vertical mode.

CPP is a technical overview of the architecture, programming languages, and support software of the Gamma II Plus series of computers. CPP, page iii. Referring to Fig. 2.1, it can be seen that the Gamma II Plus series of computers utilize an array memory as its primary storage unit. The architecture of the Gamma II Plus computer is clearly shown in Fig. 2.1. Significantly, the figure illustrates that the Master Control Unit ("MCU") is coupled in parallel with each one of the PEs which form the processor array. Similarly, each of the PEs is coupled via a 1-bit connection to its respective portion of the array memory. See page 2-10. Further, as noted on page 2-11, the MCU "... is mainly concerned with issuing instruction stream to the" PE array. CPP therefore, fails to teach or suggest a data path circuit disposed between a PE and a memory as required by independent claims 1, 11, 22, and 33. Similarly, CPP also fails to teach or suggest providing data to a data path circuit and passing that data through the data path circuit to a PE as required by independent claims 41 and 48.

The Office Action additionally cites to Fung, which is directed to a massively parallel processor computer. Rreferring to Fig. 1, Fung discloses a computer system including an array 22 of processing elements 44. The array 22 is also coupled to a CPU 29 via bus 29. Column 5, lines 4-10. Significantly, the computer system of Fung does not require conversion between vertical and horizontal modes of data storage. This is because

the computer system of Fung lacks a main memory. More specifically, the processing element 44 of Fung (shown in greater detail in Fig. 2) includes a processing circuit (comprising counter/shifter 54, logic-slider sub-unit 56, and mask sub-unit 58) which is coupled via a bidirectional single bit bus 52 to a local memory unit 50. The natural data format for each PE of Fung is therefore in the horizontal direction. As such, Fig. 2 shows no data conversion circuit interposed between the local memory unit 50 portion and the processing portion of the processing element. Indeed, since the data access performed by the general purpose CPU 26 is also in the horizontal direction, data is never needed or stored in the vertical direction in the computer system disclosed by Fung. Fung therefore fails to teach or suggest the claimed circuitry and steps recited in independent claims 1, 11, 22, 33, 41 and 48.

Claims 1, 11, 22, 33, 41, and 48 are therefore believed to be allowable over the prior art of record. Claims 2-6 (which depend from claim 1), 12-13 (which depend from claim 11), 23-27 (which depend from claim 22), 34-35 (which depend from claim 33), 43-47 (which depend from claim 41), and 49 and 51 (which depend from claim 48) are also believed to be allowable for these reasons and because the combination recited in the claims are not taught or suggested by the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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